

SYNCHRONIZATION SYSTEM, SYNCHRONIZATION METHOD AND SYSTEM

Publication number: KR20030035981 (A)

Publication date: 2003-05-09

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Classification:

- international: *G06F1/08; G06F1/12; H03L7/06; H03L7/07; H03L7/08; H04B7/26; H04L7/00; H04L7/033; H04L7/04; G06F1/08; G06F1/12; H03L7/06; H03L7/07; H03L7/08; H04B7/26; H04L7/00; H04L7/033; H04L7/04; (IPC1-7): H04B7/26*

- European: H03L7/06; H03L7/07

Application number: KR20020065824 20021028

Priority number(s): US20010021133 20011029

Also published as:

 DE10233615 (A1)
 US2003084362 (A1)
 US6836852 (B2)
 TW236580 (B)
 JP2003209539 (A)

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Abstract of KR 20030035981 (A)

PURPOSE: A synchronization system, a synchronization method and a system are provided to generate and synchronize multiple clocks having extremely low skew across multiple channels and latency that is both minimal and well-defined. **CONSTITUTION:** A TX PLL(Phase Locked Loop)(122) generates a plurality of clock signals to synchronize channel circuits(124(1)-124(N)) that receive core data streams. The channel circuits(124(1)-124(N)) convert the core data streams into serial data streams. The TX PLL(122) or a core PLL(102) generates a core clock signal for transferring the core data streams to the channel circuits(124(1)-124(N)) and registering the core data streams. One or more clock signals are distributed to the channel circuits(124(1)-124(N)) by register-to-register transfer.

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